AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-29 (canceled) Claims 1-29 were previously canceled.

30. (Currently Amended) A non-volatile semiconductor memory device having a memory transistor comprising a source region and a drain region formed ~~on~~ at a surface portion of a semiconductor while sandwiching a channel-forming region there between, a gate insulating film comprised of a tunnel insulating film, a nitride film, and a top insulating film sequentially stacked on the channel-forming region and including dispersed charge storing means in the stacked films, and a gate electrode on the gate insulating film, wherein

a thickness of said tunnel insulating film and said top insulating film are set so that the thickness of said gate insulating film converted to an oxide film becomes 10 nm or less and the change of the threshold voltage at the time of erasing said memory transistor is regulated by a recombination process of a hole current injected from said channel-forming region side and an electron current injected from said gate electrode side.

31. (Original) A non-volatile semiconductor memory device as set forth in claim 30, wherein

the thickness of said tunnel insulating film is 2.5 nm or more, and

a ratio of thickness of the top insulating film to said tunnel insulating film is 1.4 or more.

32. (Original) A non-volatile semiconductor memory device as set forth in claim 30, further comprising:

a plurality of work lines;

a plurality of common lines in the bit direction intersecting the plurality of word lines in an electrically insulated state;

a plurality of gate electrodes connected to the plurality of work lines; and

a plurality of said source regions or drain regions coupled to said plurality of common lines.

33. (Original) A non-volatile semiconductor memory device as set forth in claim 32, comprising:

a word line for commonly connecting said gate electrodes in the word direction;

a source line for commonly connecting said source regions in the bit direction; and

a bit line for commonly connecting said drain regions in the bit direction.

34. (Original) A non-volatile semiconductor memory device as set forth in claim 33, wherein

said source line comprises a sub source line for commonly connecting said source regions in the bit direction, and a main source line for commonly connecting sub source lines in the bit direction; and

said bit line comprises a sub bit line commonly connecting said drain regions in the bit direction, and a main bit line for commonly connecting sub bit lines in the bit direction.

35. (Original) A non-volatile semiconductor memory device as set forth in claim 30, wherein said dispersed charge storing means is made to be separated at least in a surface direction facing said channel-forming region.

36. (Original) A non-volatile semiconductor memory device as set forth in claim 30, wherein said dispersed charge storing means does not have conductivity over the entire

surface direction facing said channel-forming region at least when charges do not dissipate outside.

37. (Original) A non-volatile semiconductor memory device as set forth in claim 36, wherein said gate insulating film includes:

a tunnel insulating film on said channel forming region; and

a nitride film or an oxynitride film on the tunnel insulating film.

38. (Original) A non-volatile semiconductor memory device as set forth in claim 36, wherein said gate insulating film includes:

a tunnel insulating film on said channel-forming region; and

mutually insulated fine particle conductors formed on the tunnel insulating film as the above dispersed charge storing means.

39. (Original) A non-volatile semiconductor memory device as set forth in claim 38, wherein said fine particle conductors have a particle diameter of not more than 10 nm.